ABSTRACT

In a signal processing integrated circuit having an analog to digital converter and a digital filter having a plurality of taps separated in time, when starting a conversion after a reset or a change of input channel, the filter will have an incomplete set of input data as the delayed inputs to an output calculation are all zero from the reset operation. After reset, during the time that data are filling up the filter pipeline, the calculation of an output value will give a result that holds information about the input, but does not present the data with the same scaling and frequency content as the fully settled filter. The integrated circuit selectively provides two modes, on that provides only fully settled data from the filter or and another that provides all data from the filter, including unsettled data. Knowledge about the filter coefficients can be utilized by a user or user process to extract information about the input from the unsettled data.